Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **A0**
2. **N. O0**
3. **A1**
4. **N. O1**
5. **A2**
6. **N. O2**
7. **GND**
8. **N. O5**
9. **A5**
10. **N. O4**
11. **A4**
12. **N. O3**
13. **A3**
14. **VCC**

**13**

**14**

**1**

**8**

**7**

**6**

**12 11 10 9**

**2 3 4 5**

**DIE ID**

**M004U**

**M004U**

**2A**

**.056”**

**.054”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: M004U**

**APPROVED BY: DK DIE SIZE .054” X .056” DATE: 5/15/17**

**MFG: FAIRCHILD THICKNESS .015” P/N: 54F04**

**DG 10.1.2**

#### Rev B, 7/19/02